RELIABILITY REPORT

FOR

UM491

PLASTIC ENCAPSULATED DEVICES

June 20, 2009

UNION INTEGRATED PRODUCTS

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Conclusion

The UM491 successfully meets the quality and reliability standards required of all Union products. In addition, Union's continuous reliability monitoring program ensures that all outgoing products will continue to meet Union's quality and reliability standards.

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I. Device Description

A. General

The UM491 is ±15kV electrostatic discharge (ESD)-protected, high-speed transceivers for RS-422 communication that contain one driver and one receiver. The device features fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. This means that the receiver output will be a logic high if all transmitters on a terminated bus are disabled (high impedance). The UM491 offers higher driver output slew-rate limits, allowing transmit speeds up to 2.5Mbps. The device features enhanced ESD protection. All transmitter outputs and receiver inputs are protected to ±15kV using the Human Body Model. These transceivers typically draw 375µA of supply current when unloaded, or when fully loaded with the drivers disabled.

The device has a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus. The UM491 is intended for full-duplex communications.

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage (V_{CC})	+7V
Control Input Voltage (/RE, DE)	-0.3V to (V_{CC} + 0.3V)
Driver Input Voltage (DI)	-0.3V to (V_{CC} + 0.3V)
Driver Output Voltage (Y,Z)	-7.5V to 12.5V
Receiver Input Voltage (A, B)	-7.5V to 12.5V
Receiver Output Voltage (RO)	-0.3V to (V_{CC} + 0.3V)
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
14-Pin SO	471mW
Derate above +70°C	
14-Pin SO	5.88mW/°C

II. Manufacturing Information

A.	Description/Function:	±15kV ESD-Protected, Slew-Rate-Limited, Fail-Safe, RS-422 Transceiver
B.	Process:	CB12 (Standard 1.2 micron silicon gate CMOS)
C.	Number of Device Transistors:	631
D.	Fabrication Location:	Shanghai , China
E.	Assembly Location:	China
F.	Date of Initial Production:	March, 2008

III. Packaging Information

A.	Package Type:	14-Lead SO
B.	Lead Frame:	Cu (C194)
C.	Lead Finish:	Solder Plate
D.	Die Attach:	Silver-filled Epoxy
E.	Bondwire:	Gold (1.0 mil dia.)
F.	Mold Material:	Epoxy Mold Compound
G.	Assembly Diagram:	Attached Bonding Diagram
H.	Flammability Rating:	Class UL94-V0

IV. Die Information

A.	Dimensions:	1380um x 1560 um
B.	Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C.	Interconnect:	Aluminum/Si (Si = 1%)
D.	Backside Metallization:	None
E.	Minimum Metal Width:	3 microns (as drawn)
F.	Minimum Metal Spacing:	1.6microns(as drawn)
G.	Bondpad Dimensions:	4 mil. Sq.
H.	Isolation Dielectric:	SiO_2
I.	Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

B. Observed Outgoing Defect Rate: < 50 ppm

C. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 77 \times 2}$$

(Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 14.10 \times 10^{-9}$ $\lambda = 14.10$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Union's reliability qualification and monitor programs. Union also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Union performs failure analysis on lots exceeding this level. The following Burn-In Schematic shows the static circuit used for this test.

B. Moisture Resistance Tests

Union evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85 C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The UM003R1 die type has been found to have all pins able to withstand a transient pulse of ± 2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 200mA.

Table 1
Reliability Evaluation Test Results

UM491

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		77	0
Moisture Testing (Note 1)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SO	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 1)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

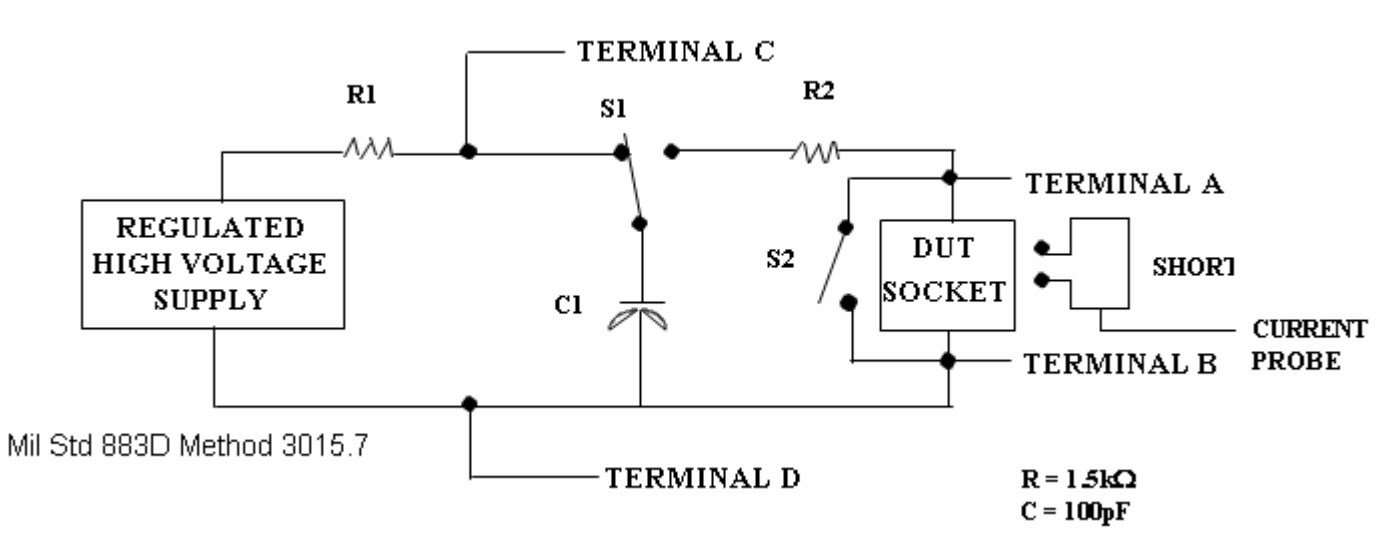
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

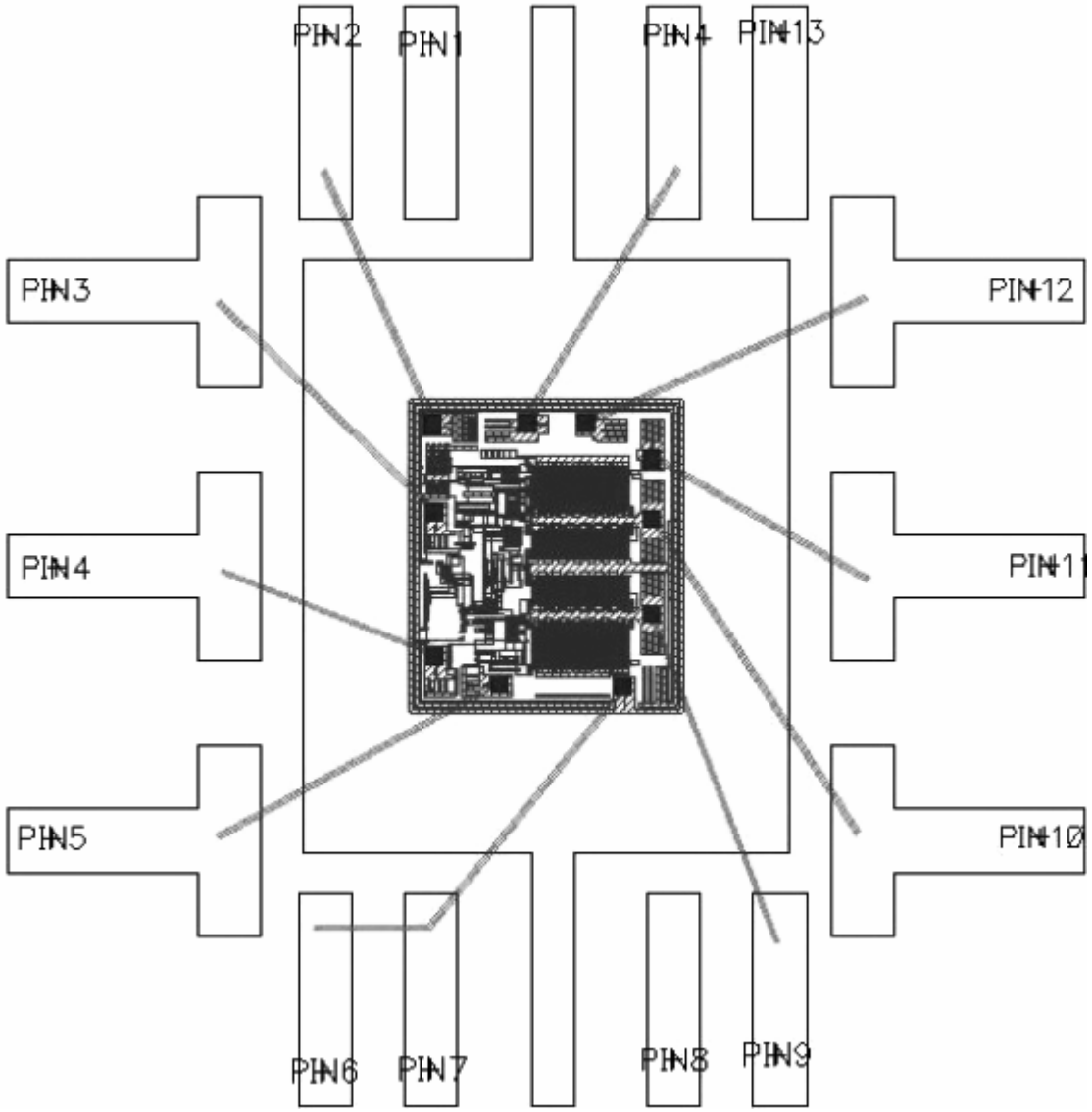
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





UM491 BONDING DIAGRAM